AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions, and listings, of claims in the application:

Listing of Claims:

1. **(Currently Amended)** A matrix converter comprising current commutation circuitry having a matrix switch arrangement including ~~with~~ a plurality of power semiconductor bi-directional switches arranged in a matrix configuration ~~to effect operation of the plurality of bi-directional switches to begin~~, said matrix switch arrangement performing timing/delay operations effecting commutation functions with initiation of one switch before de-activation of another switch wherein the ~~current commutation circuitry~~ matrix switch arrangement provides a commutation interval which approaches or equals zero.

2. **(Currently Amended)** A converter according to Claim 1 wherein the matrix switch arrangement comprises ~~comprising~~ a first switch and a second switch whereby, in a first mode in use, the first switch is activated and the second switch is not activated, and the ~~current commutation circuitry is operable to activate~~ matrix switch arrangement performs timing/delay operations which activates the second switch before the first switch is de-activated.

3. **(Currently Amended)** A converter according to Claim 1 wherein the ~~current commutation circuitry~~ matrix switch arrangement comprises circuitry performing timing/delay operations of the switches to minimize the commutation interval.

4. **(Currently Amended)** A converter according to Claim 1 wherein the ~~current commutation circuitry~~ matrix switch arrangement comprises circuitry performing timing/delay operations of the switches to provide a commutation interval of less than those typically used as a deadtime in a Voltage Source Inverter.

5. **(Canceled)**

6. **(Currently Amended)** A converter according to Claim 1 wherein the ~~current commutation interval~~ matrix switch arrangement comprises circuitry performing timing/delay operations of the switches to provide a commutation interval which is negative.

7. **(Canceled)**

8. **(Previously Presented)** A converter according to Claim 1 wherein the converter comprises the plurality of bi-directional switches configured to effect reduction of the commutation interval.

9. **(Canceled)**

10. **(Currently Amended)** A method of operating a matrix converter having a matrix switch arrangement including a plurality of power semi-conductor bi-directional switches arranged in a matrix configuration, the method comprising ~~effecting current commutation to operate the plurality of bi-directional switches to begin~~ operating said matrix switch arrangement to perform timing/delay operations effecting commutation functions with activation of ~~one~~ a first switch before de-activation of ~~another~~ a second switch wherein a commutation interval approaches or equals zero.

11. **(Currently Amended)** A method according to claim 10 wherein, in a first mode, in use, the first switch is activated and the second switch is not activated and then the matrix switch arrangement activates ~~comprising effecting the current commutation in order to activate a~~ the second switch before [[a]] the first switch is de-activated.

12. **(Currently Amended)** A method according to claim 10 ~~comprising~~ wherein the matrix switch arrangement performs/delay operations on the switch thereby minimizing the commutation interval.

13. **(Currently Amended)** A method according to claim 10 ~~comprising~~ wherein the matrix switch arrangement performs timing/delay operations on the switch thereby providing a commutation interval of less than those typically used as a deadtime in a Voltage Source Inverter.

14. **(Canceled)**

15. **(Currently Amended)** A method according to claim 10 ~~comprising~~ wherein the matrix switch arrangement performs timing/delay operations on the switch thereby providing a commutation interval which is negative.

16. **(Cancelled)**

17. **(Currently Amended)** A method according to claim 10 ~~comprising~~ wherein the matrix switch arrangement performs timing/delay operations on the switch ~~operating the plurality of bi-directional switches~~ thereby to effect reduction of the commutation interval.

18.-22. **(Cancelled)**

23. **(New)** A converter according to Claim 1 wherein the matrix switch arrangement comprises timer/delay operations of the power semiconductor bi-directional switches according to any one or more of Tables 6 to 11.

24. **(New)** A method according to Claim 10 comprising the matrix switch arrangement performing timing/delay operations of the power semiconductor bi-directional switches according to one or more of Tables 6 to 11.